

# Transmission of Timing-critical Signals Using TTL Levels

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## REVISION HISTORY

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1	2000-05-04	Draft	Johannes M. Vogt Staff Scientist

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# 1. INTRODUCTION

## 1.1 Purpose

This document specifies the use of TTL signals in timing-critical applications at the CLS, in particular the termination and biasing schemes for the inputs and outputs of devices or modules.

## 1.2 Scope

This specification is to ensure compatibility of all fast TTL inputs and outputs regarding biasing, termination, and the logic levels used. It does not guarantee performance numbers like jitter stability of attainable clock rates, since the speed of TTL inputs and outputs depends on the particular TTL IC-family that is used.

This specification does not make the use of TTL signal levels mandatory. However, when using TTL signals, it is recommended to follow the design rules defined in this specification even if timing-stability is not critical.

## 1.3 Background

TTL signal levels are commonly used to transmit signals between electronics modules or devices. The choice of TTL as a signal standard between devices is a matter of convenience, since the same signal levels are used by the most common and inexpensive family of logic ICs, thus eliminating the need to level-shift the input and output signals of these devices.

TTL signals have rise and fall times of several nanoseconds, and they would not normally be used in applications where timing stability is critical at the 1 ns level. However, if properly set up TTL circuits can achieve jitter-stabilities of better than 1 ns.

In the past (at SAL), various termination and biasing schemes have been used for TTL signal transmission. When mixed, these schemes result in reduced noise margins, or in systems, that function reliably only when connected by very short cables.

## 1.4 Definitions and Abbreviations

TTL	Transistor-transistor-logic
$V_{OH}$	TTL output "high" voltage (>2.4 V)
$V_{OL}$	TTL output "low" voltage (< 0.4 V)
$V_{IH}$	TTL input "high" voltage (> 2.0 V)
$V_{IL}$	TTL input "low" voltage (< 0.8 V)

"Input" refers to the input of a device or module, not to the input of an IC.

"Output" refers to the output of a device or module, not to the output of an IC.

## 2. Requirements

### 2.1 Function

#### 2.1.1 Logic Levels

All TTL signals shall be active-low signals.

Signal timing shall be derived from the negative-going edge of the signal, i.e. from the transition from TTL “high” to TTL “low”.

Outputs shall comply with the definition of TTL  $V_{OH}$  and  $V_{OL}$ .

Inputs shall comply with the definition of TTL  $V_{IH}$  and  $V_{IL}$ .

#### 2.1.2 Biasing

The quiescent level of any open input shall be  $> 2.4V$ , consistent with TTL  $V_{OH}$ .

Observation: This biasing requirement allows the use of open-collector output drivers.

#### 2.1.3 Termination

All devices or modules shall be set up for receiving-end termination, i.e. the input impedance shall be the equal to the characteristic impedance of the cable. Outputs do not have to be back-terminated.

Fig. 1 shows the termination scheme recommended for 50  $\Omega$  coax cable.

Fig. 2 shows the termination scheme recommended for twisted pair cable.

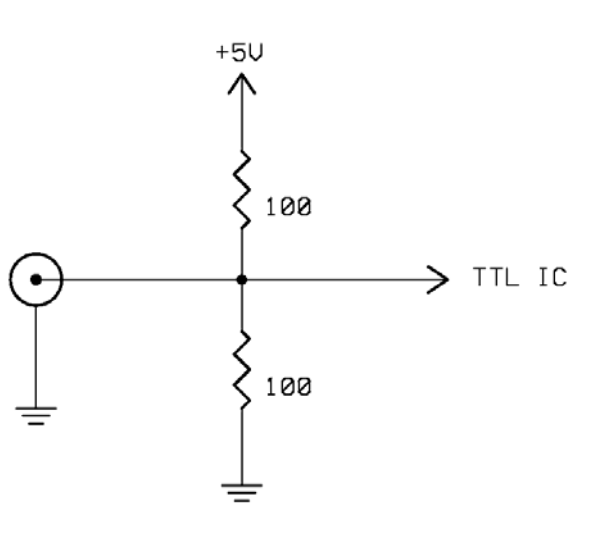


Fig. 1: Termination scheme recommended for signal transmission using 50  $\Omega$  coax cable.

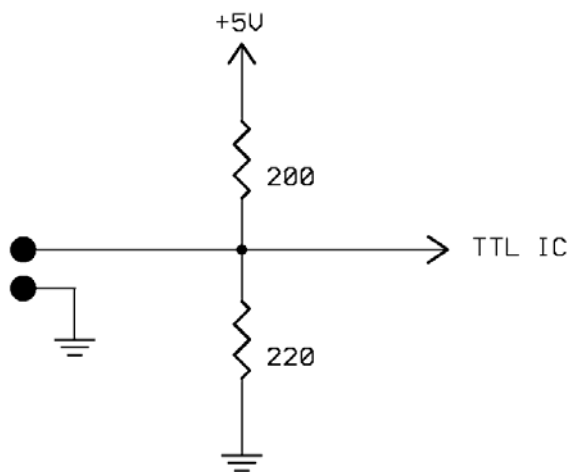


Fig. 2: Termination scheme recommended for signal transmission using twisted pair cable, carrying signal and ground.

## 2.2 Performance

The performance (attainable clock rates, jitter stability) depends on the particular TTL IC-family that is used. This document does not specify performance requirements. However, it is recommended to use one of the high performance TTL families (e.g. 74F, 74S) in all timing-critical applications.

## 2.3 Safety and Environmental

N/A

## 2.4 Applicable Codes, Standards and Procedures

N/A

## 2.5 Quality Assurance

N/A

## 2.6 Inspection, Testing and Commissioning

N/A

## 2.7 Reliability and Maintainability

N/A

## **2.8 Layout**

For best high-speed performance the input and output stages of any device should be laid out to minimize stray capacitances.

## **2.9 Vibration and Acoustic Noise**

N/A

## **2.10 Services**

N/A

## **2.11 Other Requirements and Constraints**

N/A

## **3. References**

Fairchild FAST Applications Handbook

Motorola FAST and LS TTL Data Book